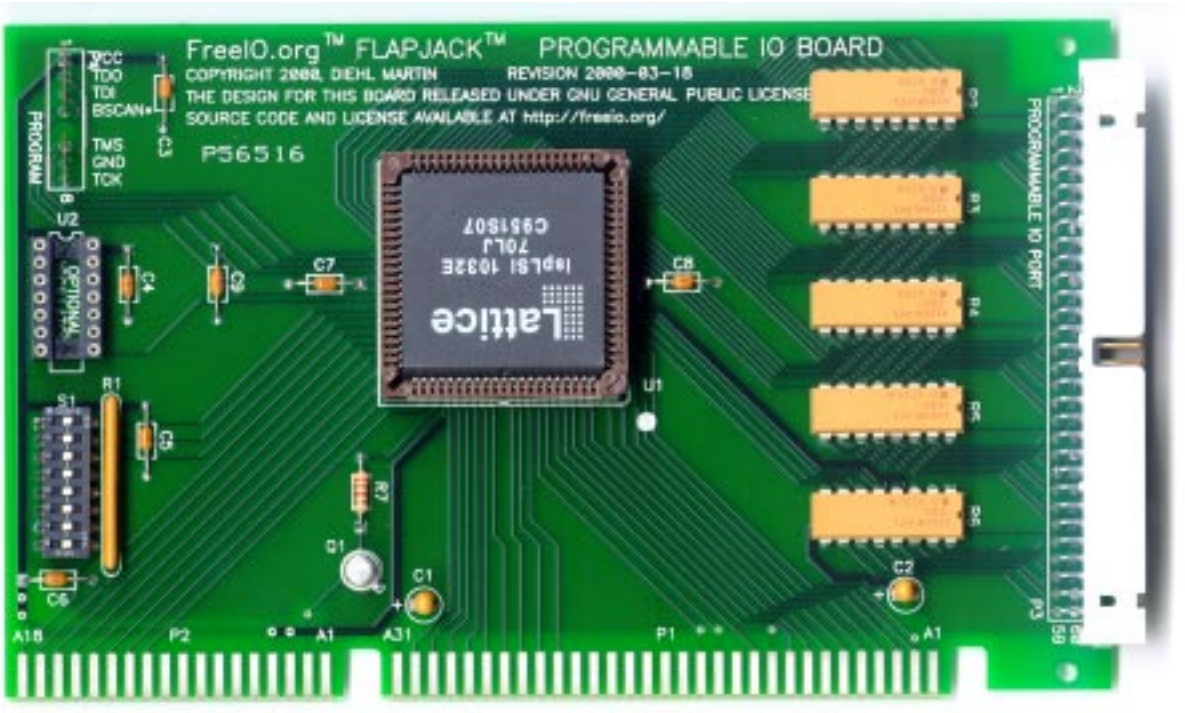
FreeIO.org(tm) Flapjack(tm) Board



Hardware Description

The hardware consists of a 16-bit ISA-bus printed circuit board designed to operate in an IBM-PC clone computer. The board measures 99 mm (3.9”) high by 157 mm (6.2”) wide and is made of 1.6 mm (0.062”) thick, double-sided, plated-through, type G-10 epoxy/glass laminated printed circuit board.

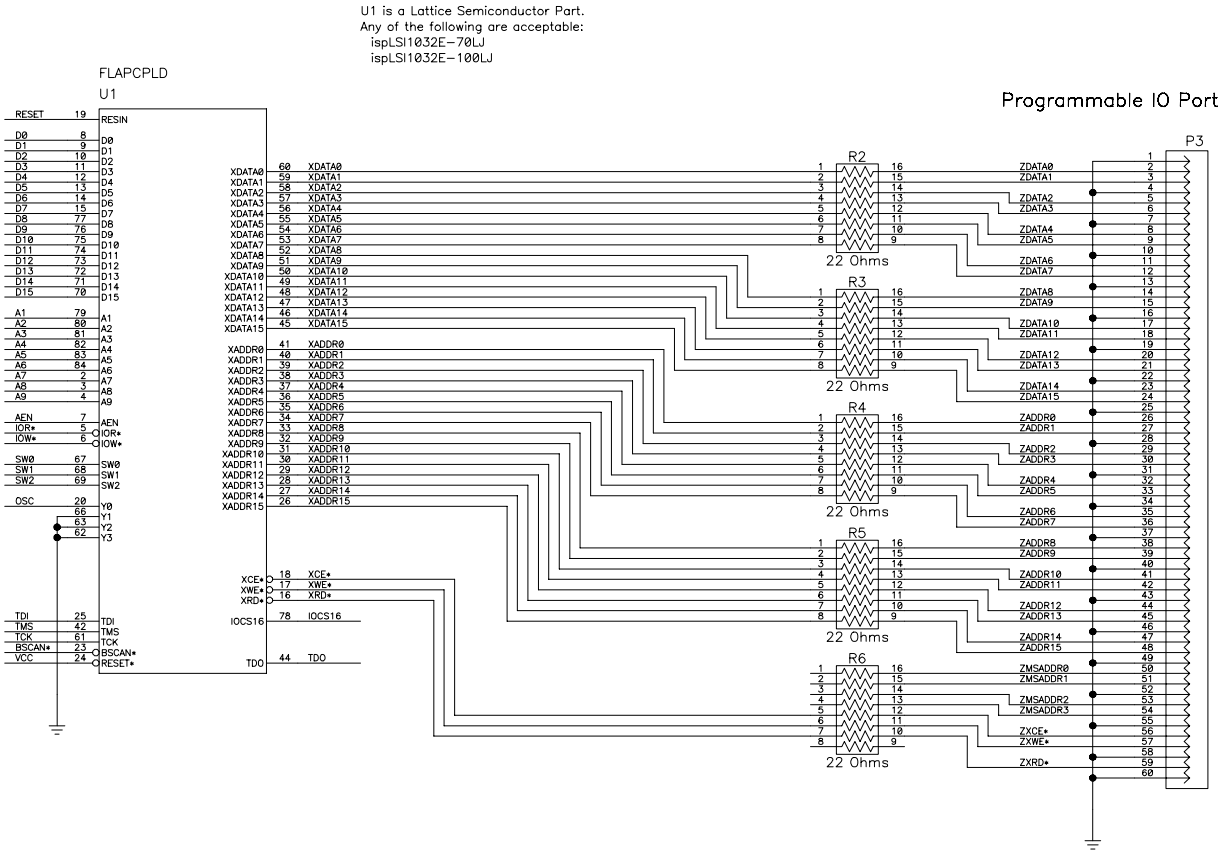
Four connectors are provided. The 62 and 36 pin edge connectors are provided for the ISA-bus connection. An 8-pin programming port is provided to allow the Complex Programmable Logic Device (CPLD) to be programmed in-place. A 60-pin input/output port carries all of the signals to and from devices outside the computer.

A continuous ground plane is provided on the bottom (solder) side of the printed circuit board. This provides a relatively constant signal impedance for the signal traces on the top of the board, and reduces the susceptibility to and emission of electromagnetic interference (EMI).

Electrical Description

The board has one active component on it, the Lattice ispLSI1032 Complex Programmable Logic Device (CPLD). This is a 5 volt part, which matches the voltage supplied by the ISA-bus

connectors. Because this is an in-system programmable part, the functionality of the board may be changed arbitrarily at any time, through programming port P4. This allows use of the board to perform functions other than those described herein, limited primarily by the dedicated ISA-bus interconnections.

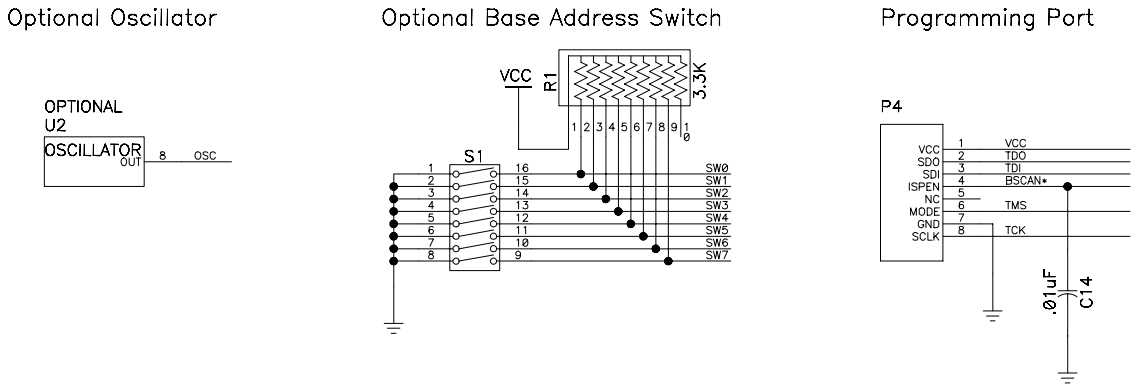


There are 35 signal lines from the CPLD connected to P4, the I/O connector. Each of these lines has a 22 ohm resistor in series with it, to form a series termination. Series terminations are used with cables of any significant length to help absorb the high-speed reflections of the signals which occur in unterminated or improperly terminated cables. The resistors are housed in resistor networks R2 - R6, each of which has eight independent resistors.

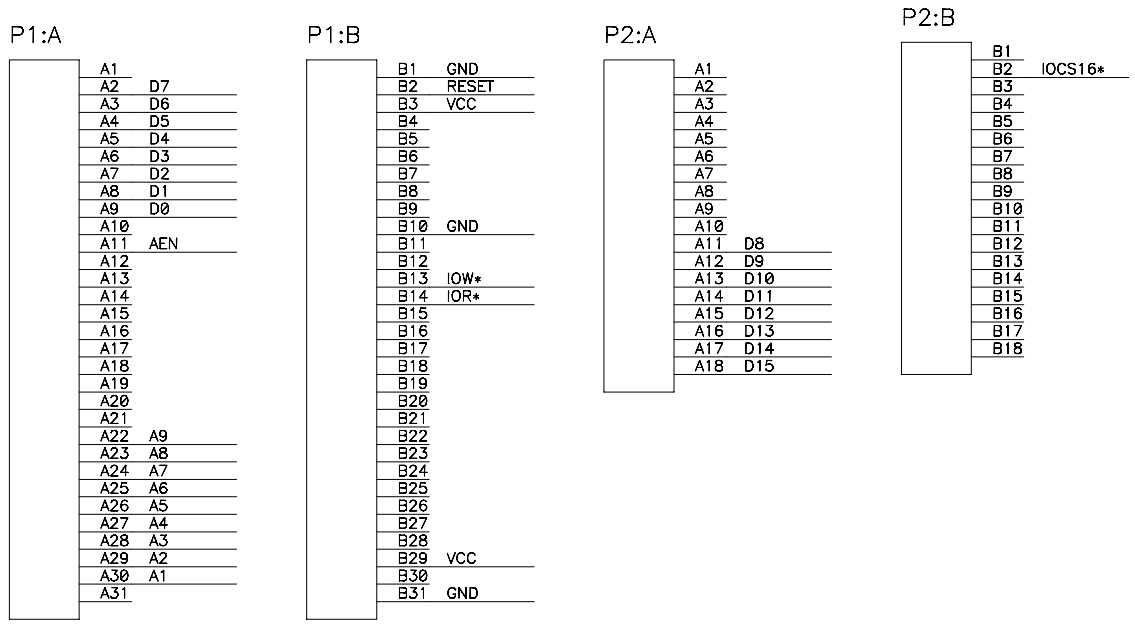
Switch S1 allows three lines from the CPLD to be switched to ground, to provide the ability to make operational selections without having to reprogram the board. The CPLD lines can be programmed as inputs which are pulled high through resistors (logic 1). The switch in the OFF position leaves the line pulled high, but in the ON position connects the line to ground, which pulls the line low (logic 0). In the supplied program, S1 is used to select the base address of the board from a selection of eight possible base addresses in I/O space.

The empty socket at U2 is for an optional oscillator. This is not needed for use with the supplied program, but may be used if a clock signal is needed for an alternative use of the CPLD. The output from the oscillator (pin 8) is connected to the primary clock input of the CPLD.

The Programming Port, P4, provides the necessary signals to program the electrically erasable programmable read only memory (EEPROM) within the CPLD, to allow its functions to be programmed. The port pinout is set to match the Lattice programming cable, which allows programming from a PC parallel port.

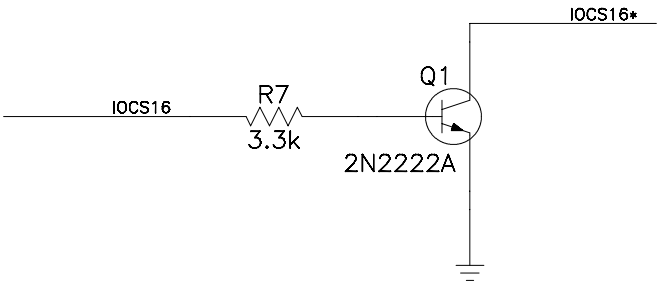


The 16-bit ISA bus connectors, P1 and P2, connect the signals from the bus to the board. Only the signals required for I/O addressed data transfers are connected.



Signals A0-A9 are the address lines; there are only ten address lines because of the IBM-PC limitation which decodes only those lines in the I/O mode. Signals D0-D15 are the bi-directional data lines. IOW* and IOR* are the negative logic I/O write and read control lines respectively. AEN is the direct memory access (DMA) enable line, which when high indicates that what appears to be an I/O action is instead a DMA cycle. IOCS16* is the open-collector negative-logic 16-bit transfer line, which the card must pull low when it is addressed in order to command

the processor to transfer the data as a single 16-bit word rather than two successive 8-bit words. Transistor Q1 is required to supply the open collector capability which the ispLSI1032 lacks.



Interface Description

The 60-pin Programmable I/O port, P4, has 35 lines which can be programmed as either inputs or outputs. In order to insure signal integrity, 4 lines are unused, and the remaining 21 pins are grounded, with no more than two signal lines between ground lines.

The basic supplied CPLD program assigns the 35 active lines as follows:

Lines ZDATA0-ZDATA15 are bi-directional connections for a 16-bit data bus.

Lines ZADDR0-ZADDR15 are output connections for a 16-bit address. This address bus provides the least significant 16 bits of a 20 bit address range.

Line ZMSADDR0-ZMSADDR3 are not used on the Flapjack board.

Line ZXCE* is a negative-logic output control signal which is driven low during any data read from, or write to, this data port.

Line ZXWE* is a negative-logic output control signal which is driven low during any data write to this data port. Data is transferred on the rising edge of the ZXWE* pulse.

Line ZXRD* is a negative-logic output control signal which is driven low during any data read from this data port. Data is transferred on the rising edge of the ZXRD* pulse.

Software Description

Using the basic supplied CPLD program, the board appears as three registers in I/O space, which are written to / read from using I/O instructions. The base I/O address is programmable in the VHDL code, and also may be further selected using optional switch S1. The I/O address ranges are as follows:

S1-3 S1-2 S1-1 Logical Address Base Address I/O Address Range

on	on	on	000	0200	0200-020f
on	on	off	001	0210	0210-021f
on	off	on	010	0220	0220-022f
on	off	off	011	0230	0230-023f
off	on	on	100	0240	0240-024f
off	on	off	101	0250	0250-025f
off	off	on	110	0260	0260-026f
off	off	off	111	0270	0270-027f

Note that these numbers can all be changed by changing the VHDL code and reprogramming the CPLD. The programmability allows great flexibility in this matter.

The three ports/registers are located as follows in I/O space in the PC:

Base Address + 0	Data word, read/write
Base Address + 2	Address word, 16 bits, write only

The address space reachable through these ports is 65,536 each 16-bit words. In order to write to or read from a device connected to the board, it is necessary to first write the address word as required, and then perform the data write/read. In this way, a 64Kx16 data space may be reached by utilizing only three I/O addresses.

Programming the CPLD

The CPLD is programmable on the board, and may be programmed while installed in a computer. During the testing of the board, it was programmed by the computer into which it was installed. During programming, all of the I/O lines on the CPLD are put in a high-impedance state with a pull-up resistor on each line.

Programming is accomplished by utilizing a program and cable provided by Lattice Semiconductor. The basic supplied CPLD program was developed in the VHDL language using the Lattice ispExpert-HDL package. This package is required only if it is desired to change the board functionality. Details are available on their web site: http://www.latticesemi.com/ .